

7/9/03

In the Specification

Please amend the specification of this application as follows:

Rewrite the paragraph at page 1, lines 7 to 9 as follows:

1  
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1  
--Serial Number 09/483,367, entitled "EMULATION SUSPEND MODE WITH DIFFERING RESPONSE TO DIFFERING CLASSES OF INTERRUPTS" claiming priority from U.S. Provisional Application No. 60/120,809 filed February 19, 1999, now U.S. Patent No. 6,553,513;--

Rewrite the paragraph at page 1, lines 10 to 11 as follows:

2  
2  
2  
--Serial Number 09/481,852, entitled "EMULATION SUSPENSION MODE WITH STOP MODE EXTENSION" claiming priority from U.S. Provisional Application No. 60/120,809 filed February 19, 1999, now U.S. Patent No. 6,567,933;--

Rewrite the paragraph at page 1, lines 12 to 13 as follows:

3  
3  
3  
--Serial Number 09/483,568, entitled "EMULATION SUSPEND MODE HANDLING MULTIPLE STOPS AND STARTS" claiming priority from U.S. Provisional Application No. 60/120,809 filed February 19, 1999, now U.S. Patent No. 6,564,339;--

Rewrite the paragraph at page 1, lines 14 to 15 as follows:

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4  
4  
--Serial Number 09/483,697, entitled "EMULATION SUSPEND MODE WITH FRAME CONTROLLED RESOURCE ACCESS" claiming priority from U.S. Provisional Application No. 60/120,809 filed February 19, 1999, now U.S. Patent No. 6,557,116;--

Rewrite the paragraph at page 19, line 18 to page 20, line 2 as follows:

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--Example module 200 illustrated in Figure 8 may also transit data via this alternate data transfer protocol. Programmable digital processor core 200 220 loads the data to be transmitted to

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data register OUT 212. Programmable digital processor core 200 220 then triggers start bit generator 213 and selected a data transmission mode at output switch 202. Start bit generator 213 produces the start bit which is selected for transmission to the TDO line by output switch 202. Output switch 202 then selects data register OUT 212 for serial transmission of the predetermined number of bits. This scheme is similar to that of a universal asynchronous receiver/transmitter (UART) with start bits and fixed length data. Note that the data transmitted to module may be data to be loaded into selected locations within the module or it may be instructions for execution by programmable digital processor core 220.--